Remarks

Claims 1, 2, 6, 9, 10, 13, and 16 are currently amended. Claim 5 is canceled. Claims 3, 4, 7, 8, 11, 12, 14, and 15 are original.

103(a) Rejections:

The Examiner has rejected claims 1-16 "under 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted Prior Art (hereinafter AAPA)." Claims 1 through 16 were rejected based on the allegation that applicants' prior art teaches all of the limitations recited in the claims. For example, in original independent claim 1, the Examiner maintains that "[w]ith regards to claim 1, AAPA teaches a serial peripheral interface apparatus [fig 1], comprising: a plurality of serial data-transfer means …; buffer means …; counter means …; and control means …" where all elements of claim 1 are cited as corresponding to elements taught in the cited prior art. Similar arguments were made by the Examiner for original independent claims 9 and 16 as well as original dependent claims 2-8 and 10-15.

The Present Claimed Invention:

Amended independent claim 1 is for a serial peripheral interface apparatus, comprising a plurality of serial data-transfer means coupled together for transferring data serially; a parallel data-transfer means serving as a parallel slave, the parallel data-transfer means coupled to an output of one of said plurality of serial data-transfer means; a buffer means coupled to said plurality of serial data-transfer means for storing a subsequent data byte to be transferred; a counter means coupled to said buffer means and said plurality of serial data-transfer means for checking a status of a data transmission within said serial peripheral interface apparatus; and a control means coupled to said

buffer means, said counter means, and said plurality of serial data transferring means for controlling said data transmission within said serial peripheral interface apparatus and for enabling a loading of said subsequent data byte into said buffer means by said control means reviewing a status of said counter means and a status of said buffer means.

Amended independent claim 9 is for a serial peripheral interface apparatus, comprising a plurality of shift registers coupled together for transferring data serially; a parallel slave shift register coupled to an output of one of said plurality of shift registers; a write buffer coupled to said plurality of shift registers; a bit counter coupled to said plurality of shift registers for keeping track of a bit field of a data byte being transferred through said apparatus; and a finite state machine controller coupled to said apparatus for controlling data transmission therethrough and for enabling a loading of a subsequent data byte into said write buffer by checking a status of said bit counter and a status of said write buffer.

Amended independent claim 16 is for a microcontroller comprising a central processing unit; a bus interface coupled to said central processing unit; a memory module coupled to and in communication with said central processing unit via said bus interface; a serial peripheral interface module coupled to said memory module and said bus interface; said serial peripheral interface further comprising a serial master shift register, a serial slave shift register coupled to an output of said serial master shift register for transferring data serially, and a parallel slave shift register coupled to said output of said serial master shift register; a write buffer coupled to an input of said serial slave shift register; a bit counter coupled to said serial peripheral interface module for keeping track of a data set being transferred therethrough; and a finite state machine controller coupled to said serial peripheral interface module

for controlling data transmission therethrough and for enabling a loading of a subsequent data byte into said write buffer by providing the status of said bit counter and a status of said write buffer back to said central processing unit.

Note that all amended independent claims now have both a write buffer and a parallel slave shift register.

Discussion:

The Examiner has noted on page 6 of the present Office Action that applicants' claimed invention differs from the cited prior art by incorporation of the second parallel write buffer (element 250) which is coupled to a plurality of serial shift registers.

The Examiner's arguments appear to have confused "buffer means" (claim 1) and "a write buffer" (claim 9) with the parallel slave register (element 230) presented in dependent claims 5 and 10. The Examiner's arguments reject the "buffer means" (original independent claim 1) and the parallel data-transfer means serving as a parallel slave" (original dependent claim 5) as though the two claim elements are identical, yet they are not. The Examiner's arguments further reject the "write buffer" (original independent claim 9) and the "parallel slave shift register" (original dependent claim 10) as though the two elements are considered the same element in cited prior art. The parallel slave register (element 230) was originally presented in dependent claim 5 as "a parallel data-transfer means serving as a parallel slave." The parallel slave register (element 230) was originally presented in dependent claim 10 as "a parallel slave shift register." Each of these originally claimed parallel slave shift registers is different from the new write buffer (element 250) introduced originally in independent claims 1 and 9.

To resolve references in the present claims to the parallel slave register (element 230) from references to the second parallel write buffer (element 250), original independent claim 1 is amended to additionally incorporate "a parallel data-transfer means serving as a parallel slave" (formerly of original claim 5) as the parallel slave register (element 230). Original independent claim 9 is amended to additionally include the parallel slave register (element 230) as "a parallel slave shift register" (formerly of original claim 10). Presently, amended independent claim 1 includes both "a buffer means" as a claim element representing the second parallel write buffer (element 250) and the claim element "a parallel data-transfer means" as the parallel slave register (element 230). Amended independent claim 9 includes "a write buffer" representing the second parallel write buffer (element 250) with "a parallel slave shift register" as the parallel slave register (element 230). As amended, both independent claim 1 and independent 9 contain both the second parallel write buffer (element 250) juxtaposed with the parallel slave register (element 230).

The concurrent incorporation of the phrase "buffer means" (element 250) and the phrase "parallel data-transfer means" (element 230) in amended independent claim 1 clarifies the configuration of the serial peripheral interface apparatus to contain both elements and distinguishes the apparatus over the prior art. Likewise, incorporation of the phrase "a write buffer" (element 250) concurrent with the phrase "a parallel slave shift register" (element 230) in amended independent claim 9 similarly distinguishes the claim over the cited prior art. The prior art lacks the second parallel write buffer (element 250). Amendments to the independent claims provide clarification regarding previous references to "buffer means" (original claim 1) and "write buffer" (original claim 9) from being misinterpreted as the parallel slave register (element 230). Dependent claim 5 is canceled and claim 10 is currently

amended to support presentation of the parallel slave register (element 230) in the independent claims.

Independent claim 16 claims "a parallel slave shift register" and "a write buffer" as originally presented and is amended only for correction of antecedent basis in regard to coupling. Since both the "parallel slave shift register" and "a write buffer" are originally presented, claim 16 is distinct from the prior art for at least the same reasons as presented supra.

Conclusion:

Clarification of the use of the parallel write buffer (element 250) and the parallel slave register (element 230) in the amended independent claims 1,9, and 16 avoids reading on the prior art. Clarification in usage between the two elements makes the Examiner's arguments moot. It is believed that the dependent claims 2-4, 6-8, and 10-15 as amended, are allowable by depending from allowable amended independent claims 1, 9, and 16.

Applicants believe that all of the claims in the present application are in condition for allowance and such allowance is respectfully requested. Applicants respectfully request that a timely Notice of Allowance be issued in this case.

CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signed: Sally Azevedo

Typed Name: Sally Azevedo

Date: December 23, 2005

Respectfully submitted,

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